Abstract

A feed forward clock and data recovery unit for recovering a received serial data bit stream having a feed forward phase tracking means for tracking of a sampling time to the center of a unit interval (UI) of the received data bit stream, wherein the feed forward phase tracking means comprises: sampling phase generation means for generating equidistant sample phase signals which are output with a predetermined granularity; an oversampling unit (OSU) for oversampling the received data bit stream with the sample phase signals according to a predetermined oversampling rate (OSR); a serial-to-parallel-conversion unit which converts the oversampled data stream into a deserialized data stream with a predetermined decimation factor (DF); a binary phase detection unit (BPD) for detecting an average phase difference (AVG-PH) between the received serial data bit stream and the sample phase signal by adjusting a phase detector gain (PDG) depending on the actual data density (DD) of the deserialized data stream such that the variation of the average phase detection gain (PDG) is minimized; and a loop filter for tracking of small phase offset of the detected average phase signal (AVG-PH) around an ideal sampling time at the center of the unit interval (UI) to generate a fine track control signal; a finite state machine (FSM) which detects whether the average phase signal has exceeded at least one predetermined phase threshold value and which generates a corresponding coarse shift control signal; a binary rotator which rotates the deserialized data bit stream in response to the coarse shift control signal and in response to the fine track control signal; data recognition means (DRM) for recovery of the received data stream which includes a number of parallel data recognition FIR-Filters, wherein each data recognition FIR-Filter comprises: a weighting unit for weighting data samples of the deserialized data stream which has been adjusted to the ideal sampling time by the binary rotator; a summing unit for summing up the

weighted data samples; and a comparator unit for comparing the summed up data samples with a threshold value to detect the logic value of a data bit within the received serial data bit stream.

(Figure 4)